

A STUDY OF HIGH-SPEED ANALOG-COMPUTER PERFORMANCE (THE ASTRAC I SYSTEM PERFORMANCE)*

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ABSTRACT

Increased interest in high-speed hybrid analog/digital computation has led to the development of the Arizona Statistical Repetitive Analog Computer (ASTRAC I), which employs inexpensive digital logic to control a high-speed repetitive analog computer. The design of the machine has been described elsewhere; this paper reports the results of the error analysis performed on the linear analog computing elements and digital timing circuits. The results are of particular interest for the design of new computing systems of this type.

The results of several statistical experiments are also included to further illustrate the operation and application of the various ASTRAC I computing elements.

Introduction to the ASTRAC I Computer.

The Arizona Statistical Repetitive Analog Computer (ASTRAC I, fig. 1), described in detail in references [3, 5, 6, 7, 8, 9, 11, 13, 17, 21, 24 and 32], combines

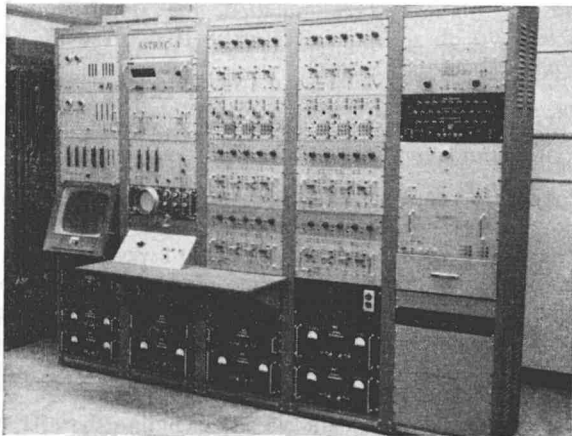


Fig. 1. — The ASTRAC Computer.

a new fast memory-equipped repetitive/iterative analog computer with digital logic and control. The resulting synthesis of high-speed analog computation with digital automatic programming is of particular interest in connection with Monte-Carlo-type studies of random processes, which serve to illustrate ASTRAC I system operation in figure 2 [4, 41].

Referring to figure 2, an analog-computer simulated control system, communications system, queuing problem, etc., is supplied random inputs, initial conditions, and/or random parameters from noise generators with Gaussian or statistically known random outputs. Reset pulses from a simple digital control unit cause repetitive

simulation of the process under study between 10 and 100 times per second at computing frequencies of 10 to 10,000 radians per second. Accurate sample-hold (analog memory) units read selected process variables at push-button preset times t_1 and t_2 seconds after the start of each computer run. A hybrid analog/digital statistics computer accepts these samples to compute statistical averages over 100 to 9900 computer runs, as determined by a preset run counter in the control unit. In this manner, one can estimate ensemble averages such as mean-square error, correlation functions, and probabilities for very complicated non-stationary as well as stationary random processes.

While the ASTRAC I system is intended mainly for an academic program of graduate instruction and re-

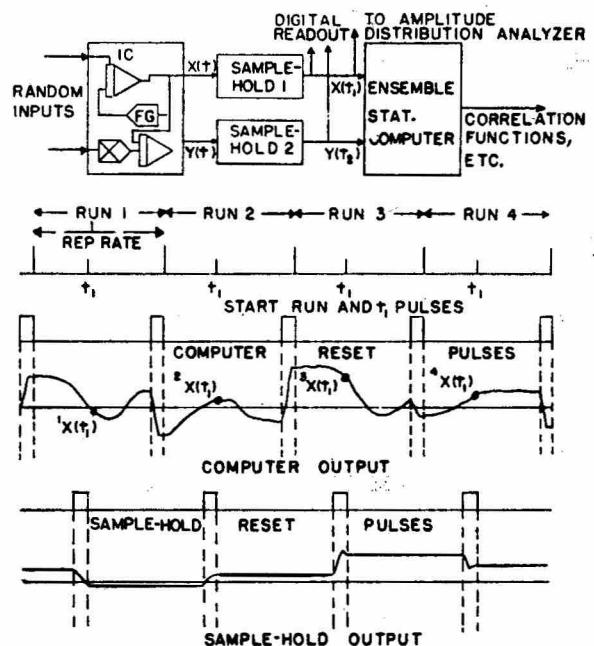
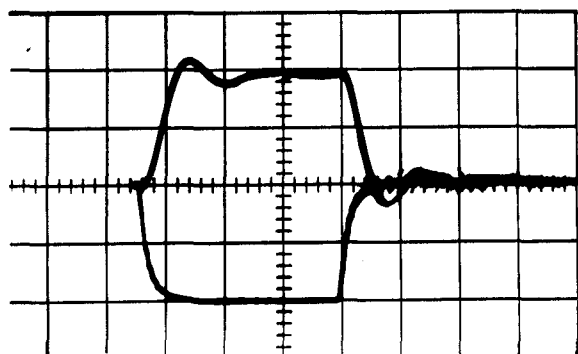


Fig. 2. — A typical repetitive-analog-computer set up together with four sample computer runs.

* Manuscript received September 27, 1963.

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Ver. scale 5 volts/cm.
Hor. scale 1 usec./cm.

2

H

Compensated phase inverter pulse response.

Fig. 6. — Oscilloscope photograph of the compensated and uncompensated inverter pulse response.

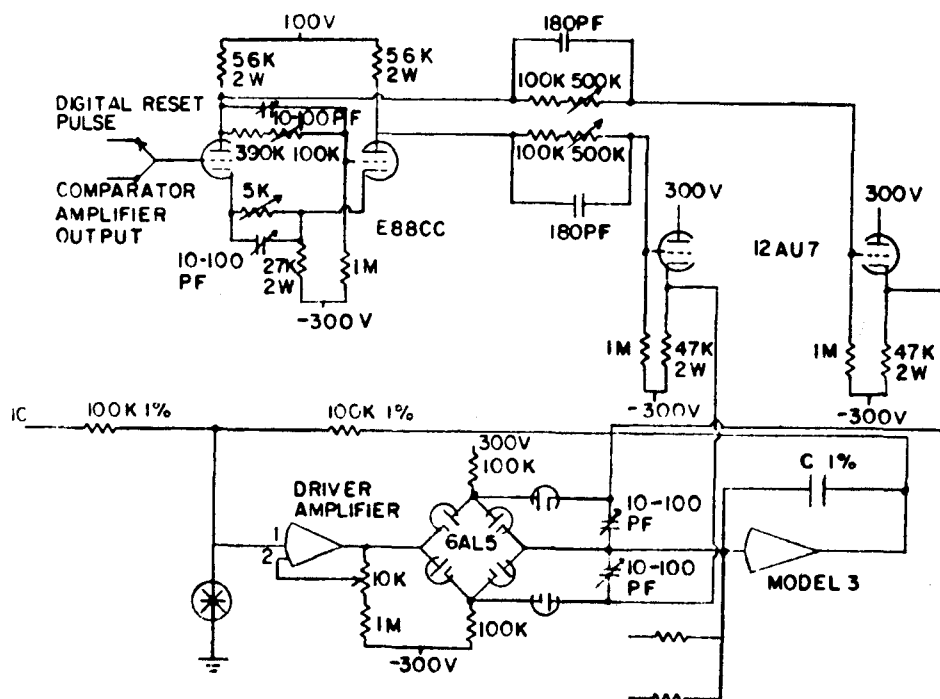


Fig. 7. — ASTRAC 1 electronically reset integrator or sample-hold circuit. For integrators the driver amplifier is a Philbrick K2-XA. For sample-hold circuits the cathode follower resistors are $33\text{K}\Omega$ the bridge resistors $33\text{K}\Omega$ and the driver amplifier is a University of Arizona Model 2 with 10 ma output current.

and solving equations (1) and (2) for $E_0(s)$ gives

$$E_0(s) = \frac{-E_1(s) - E_2(s) R_s (R + 2 R_{in}) / R_2 R_{in}}{1 + \frac{s C R_s (R + 2 R_{in})}{R_{in}} + \frac{s C R_s (R + 2 R_{in})}{A(s) R_{in}} + \frac{(R_2 + R_s) (R + 2 R_{in})}{A(s) R_2 R_{in}}} \quad (4)$$

Equation (4) can now be separated into two parts to study the effective rejection of $E_2(s)$ and the tracking response to $E_1(s)$.

If $E_1(s)$ is zero, equation (4) can be approximated at low frequencies by

$$E_0(s) \approx -E_2(s) \frac{R_s (R + 2 R_{in})}{R_2 R_{in}} \quad (5)$$

Furthermore, for $R_s \ll R_{in}$ and $R \leq R_2$, equation (5) can be again approximated to give

$$E_0(s) \approx -E_2(s) \frac{2 R_s}{R_2} \quad (6)$$

In the time domain,

$$E(t) \approx -E_2(t) \frac{2 R_s}{R_2} \quad (7)$$

In ASTRAC I, R_2 is 100K Ω or 500K Ω and the value of R_s is found by measuring $E_0(t)$ for a known $E_2(t)$

$$E(j\omega) = -E_1(j\omega) \left\{ 1 + \frac{(R_2 + R_s) (R + 2 R_{in})}{A_0 R_2 R_{in}} - \frac{\omega C R (R + 2 R_{in}) \delta_A(\omega)}{A_0 R_{in}} \right. \\ \left. - j\omega \left[\frac{C R_s (R + 2 R_{in})}{R_{in}} + \frac{C R_s (R + 2 R_{in})}{A_0 R_{in}} + \frac{(R_2 + R_s) (R + 2 R_{in}) \delta_A(\omega)}{\omega A_0 R_2 R_{in}} \right] \right\}^{-1} \quad (9)$$

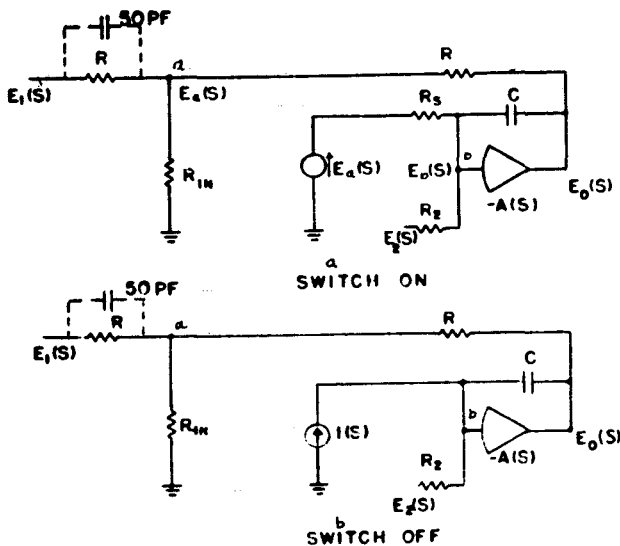


Fig. 8. — Equivalent circuit for an electronically reset integrator.

The measured frequency response with the 50 pf input compensating capacitor included, is shown in figure 9.

Equations (7) and (9) indicate that for good rejection and frequency response the switch impedance should be low, the driver input impedance high, and the

and applying equation (7). For practical purposes, the driver amplifier output impedance is zero which makes R_s equal to the switch impedance, which in general is non-linear. The value of R_s was found to be equal to or less than 300 ohms, which corresponds to a maximum value of 310 ohms taken from a linear approximation to the diode curves. The maximum rejection error is then ± 0.6 volts for each 100K Ω input and ± 0.12 volts for each 500K Ω input.

In the steady state, the open-loop amplifier gain can be written

$$A(j\omega) = \frac{A_0}{1 + j \delta_A(\omega)} \quad (8)$$

where A_0 is the d-c gain and $\delta_A(\omega)$ is, in general complex, but usually proportional to ω over a wide range of frequencies (fig. 4).

For $E_2(s)$ equal to zero and for a sinusoidal input, substitution of equation (8) into equation (4) gives the steady state gain equation

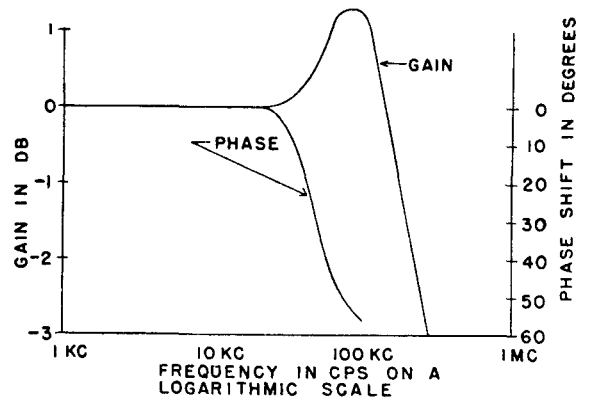


Fig. 9. — Frequency response of a gain of 1 electronically reset integrator or sample-and-hold circuit in TRACK.

operational amplifier bandwidth and gain should be as high as possible.

Although the use of either the K2-XA or the Model 2 as the driver amplifier results in the same small-signal frequency response, their current outputs for charging the capacitor are not the same and must be considered when investigating the dynamic characteristics of integrators and sample-and-hold circuits in RESET or TRACK. For a sinusoidal input

$$E_1(t) = E \sin \omega t \quad (10)$$

the voltage-current relation for a capacitor can be used to find the maximum tracking frequency for a given amplitude E . In equation form

$$f = \frac{i}{2\pi CE} \quad (11)$$

where i is the smallest current output of the driver or operational amplifier, E is the amplitude of the input sine-wave, and C is the value of the integrating capacitor. The theoretical and experimental results coincide very well and are shown in figure 10 for $C = 0.005 \mu\text{f}$.

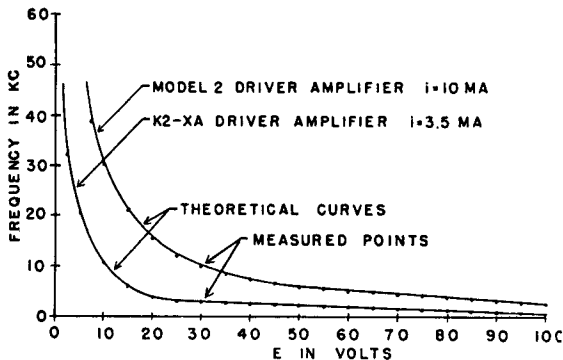


Fig. 10. — Amplitude-frequency response of electronically reset integrators and sample-hold circuits with current as a parameter.

From this, the sample-hold circuits can be said to track at 2×10^6 volts per second and the integrators at 7×10^5 volts per second.

With the switch OFF, the equivalent circuit is shown in figure 8 b. Here, the constant current generator corresponds to the switch leakage current and causes the capacitor to charge or discharge at a constant slow rate during COMPUTE or HOLD. For $C = 0.005 \mu\text{f}$, the circuit will hold within 50 mv for 100 msec. More accurate holding can be obtained at the expense of frequency response by using a larger capacitor.

4. Integrator Drift, Offset, and Switching Errors.*

D-c drift, d-c offsets, switching delays, switching offsets, and switching transients are sources of error in electronically reset integrators, and must be minimized for accurate simulation work.

The d-c drift of the integrators is less than ± 20 mv after a warm up periode of 15 minutes. D-c offsets are balanced out with a potentiometer and normally are

* Writers Note. There have been questions as to what integrator drift and offset mean in electrically reset integrators and I wish to clarify this.

The d-c offset of an electronically reset integrator is caused by a d-c offset in the switch when the switch is ON. This causes a d-c offset or initial condition error to appear at the output of the integrator. When the switch turns OFF the integrator then starts to operate from its initial condition which includes the offset error. Now if the integrator uses a chopper stabilized d-c amplifier, the major error source in COMPUTE comes from switch leakage current for which the error per unit time is given on page 15. (Note: The offset only causes error in following integrators, and this is the same as an initial condition error.)

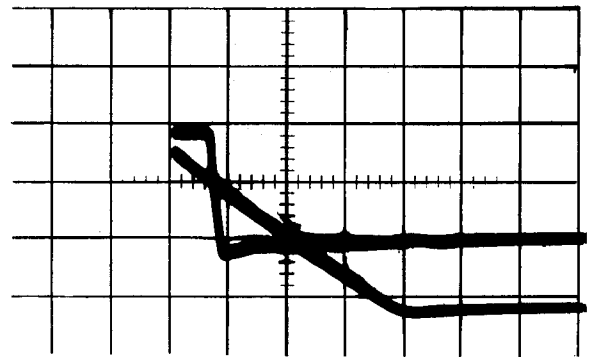


Fig. 11. — Schmitt trigger response to the computer reset pulse. The fast pulse is the Schmitt trigger output.

Ver. scale 20 volts/cm.
Hor. scale 5 usec./cm.

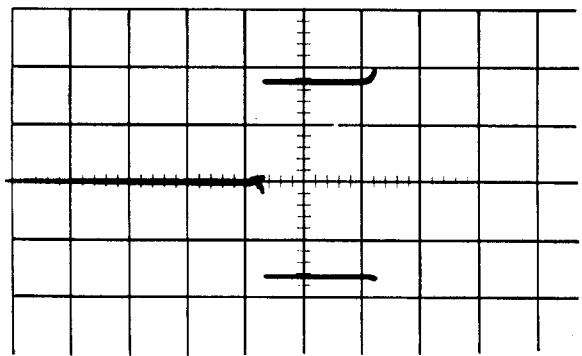


Fig. 12. — Push-pull pulses for the control of the electronic switch. For clarity, the d-c levels have been set to show one pulse above the other.

Ver. scale 20 volts/cm.
Hor. scale 0.5 msec./cm.

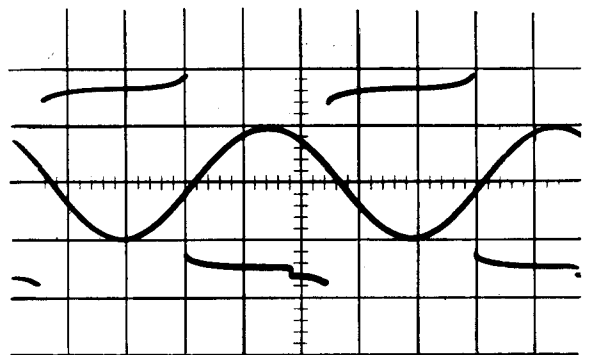


Fig. 13. — Schmitt trigger response to a sine-wave.

Ver. scale for the pulses 20 volts/cm.
Ver. scale for the sine-wave 0.5 volts/cm.
Hor. scale 0.2 msec./cm.

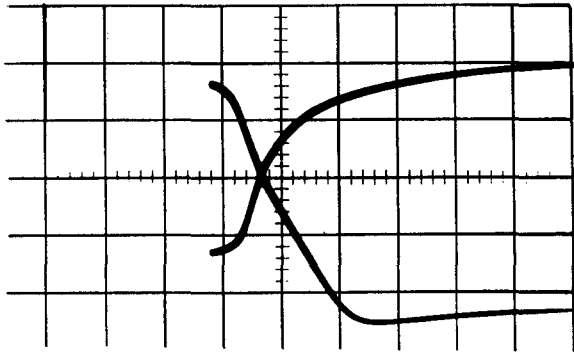
held within ± 50 mv over a two week period with no adjustment.

Figure 11 shows an oscilloscope photograph of the computer reset pulse and one side of the corresponding Schmitt trigger response.

Figure 12 is a photograph of the resulting push-pull pulses, which drive the electronic switch. The Schmitt triggers all switch at about zero volts (fig. 13), and the

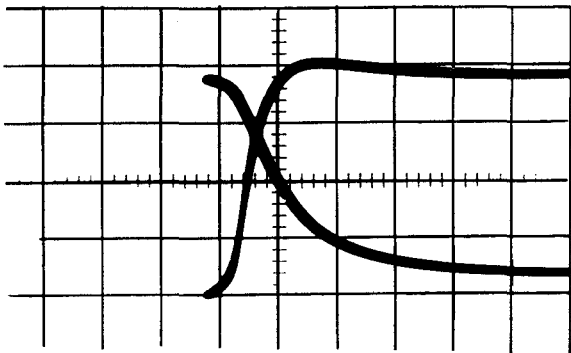
switching delay between the various integrators is less than $0.5 \mu\text{sec}$. Consequently, the effects of integrator switching delay are so small that they are masked by the normal switching transients.

After being adjusted to give zero switching offset at the integrator output, the rise and fall times of the switch control pulses are shown in figure 14. Note



Ver. scale 10 volts/cm.
Hor. scale 0.5 usec./cm.

a
Computer into RESET.



Ver. scale 10 volts/cm.
Hor. scale 0.5 usec./cm.

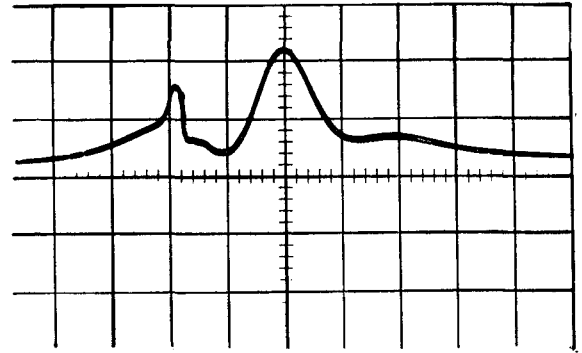
b
Computer into COMPUTE.

Fig. 14. — Rise and fall times of the switch control pulses.

that the pulses cross zero at exactly the same time going into RESET, which indicates that the electronic switch is turning ON symmetrically. This is not the case going into COMPUTE, and the difference is due to a non-symmetrical turn-off characteristic in the particular switch. In practice, the control pulses for each switch are adjusted separately to give zero switching offset and further adjustment is required about once a month to compensate for component aging.

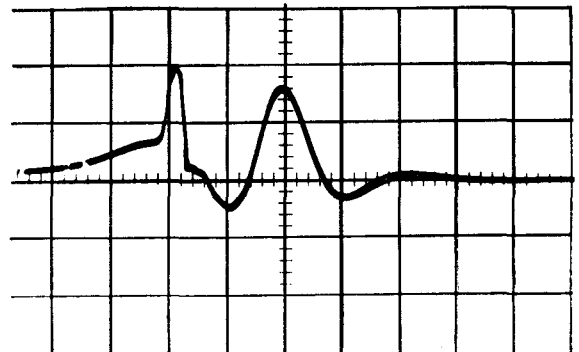
Transients at the integrator output are caused by the switching action; and their amplitude depends on the value of the integrating capacitor. When computing, these transients ride on top of the computer solution and usually contribute a small d-c error after they are damped out. Figure 15 is a photograph of typical integrator switching transients with $C = 0.01 \mu\text{f}$. For values of C up to $0.001 \mu\text{f}$, the transients increase to a maximum value of 200 mv. However, in each case they are damped to less than 50 mv in about $2 \mu\text{sec}$.

Due to a better dynamic response, the transients in the sample-hold circuits have a maximum value of 400 mv and also damp out in about $2 \mu\text{sec}$.



Ver. scale 50 mv/cm.
Hor. scale 0.5 usec./cm.

a
Computer into RESET.



Ver. scale 50 mv/cm.
Hor. scale 0.5 usec./cm.

b
Computer into COMPUTE.

Fig. 15. — Switching transients at the output of an electronically reset integrator.

5. Integrator Response to a Step Function.

Although integrators do not, strictly speaking, operate in static modes, a quasi-static integrator test consisted of measuring the integrator response to a 5 volt step function (rate test). The computer setup is shown in figure 16. The integrator output was sampled every 10 msec, and the digital voltmeter was used to read the sample value. For readout accuracy, the memory pair used for readout was calibrated within 50 mv.

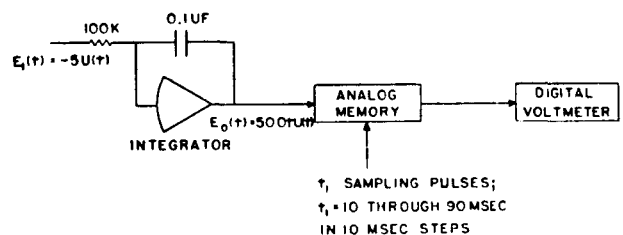


Fig. 16. — Computer setup for integrator rate test.

The test was run over all possible 100KΩ integrator inputs and the results are tabulated in table 1.

6. Dynamic Errors in Linear Computing Loops.

Dynamic errors in computer setups for the solution of linear, constant coefficient, differential equations, can be described in terms of perturbations of the characteristic roots and generation of extraneous roots. The modes of operation due to the extraneous roots are usually strongly damped, and the characteristic root perturbations alone, can be used as a measure of dynamic errors in linear computing elements. These perturbations, which are caused mainly by phase shift, show up especially well in sinusoidal solutions. (This does not necessarily mean that the percentage errors are higher in sinusoidal solutions; it only means they are easier to see). The well known harmonic oscillator computer setup (fig. 17), for the solution of the differential equation

$$\frac{d^2 x}{dt^2} = -\omega^2 x \quad (12)$$

demonstrates such a situation and serves as a sensitive test for the phase shift in linear computing elements (circle test). Writing the characteristic equation of equation (12) in Laplace form gives

$$s^2 + \omega^2 = 0 \quad (13)$$

and permits the classical representation of the characteristic roots as

$$s_{1,2} = \pm j\omega. \quad (14)$$

For $X(0) = B$ and $\dot{X}(0) = 0$, the solution of equation (12) is

$$x(t) = B \cos \omega t. \quad (15)$$

Table 1
INTEGRATOR RATE TEST

Note : The integrator rate test was run by patching — 5 volts d-c into all 36 of the 100K integrator inputs.

Sampling time in msec.	Theoretical value in volts	Average value in volts	Average error in volts	Maximum error in volts
10.0	5.0	5.1	—0.1	0.2
20.0	10.0	10.0	0.0	—0.3
30.0	15.0	15.2	—0.2	0.2
40.0	20.0	20.1	—0.1	—0.3
50.0	25.0	25.0	0.0	0.4
60.0	30.0	29.9	0.1	0.4
70.0	35.0	34.9	0.1	—0.4
80.0	40.0	39.8	0.2	0.6
90.0	45.0	44.7	0.3	0.7

The actual computer solution has a characteristic equation of the form

$$s^2 + 2\delta\omega_n s + \omega_n^2 = 0 \quad (16)$$

with roots

$$s_{1,2} = -\delta\omega_n \pm j\omega \quad (17)$$

where

$$\omega_n^2 (1 - \delta^2) = \omega^2 \quad (18)$$

and ω is the natural frequency with no damping. Normally, the magnitudes of the real parts of the roots are much smaller than the magnitudes of the imaginary parts, and ω is approximately equal to ω_n . If this is the case, the characteristic roots can be written

$$s_{1,2} = -\delta\omega \pm j\omega. \quad (19)$$

In analog computers, δ is a function of ω and for $x(0) = B$ and $\dot{x}(0) = 0$, the actual computer solution is approximately

$$x(t) = B e^{-\omega\delta(\omega)t} \cos \omega t. \quad (20)$$

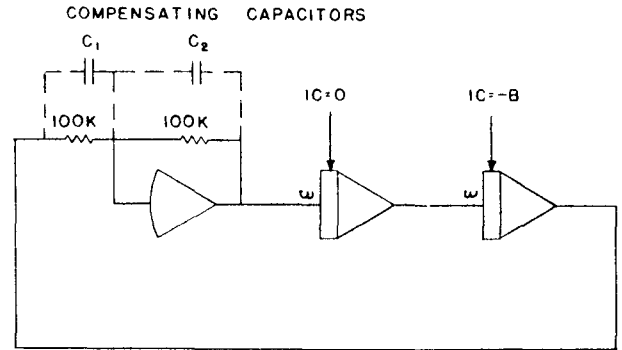


Fig. 17. — Harmonic oscillator computer setup.

It is interesting to note that, since $\delta(\omega)$ is caused by phase shift, it can be either positive or negative; in most computers, the sign may change, possibly more than once, over the frequency range of the computer [35].

Figure 18 is a plot of $\delta(\omega)$ for ASTRAC I simulations of equation (12). For demonstration purposes, the simulation was run using various compensating capacitors connected in parallel with the inverter resistors. This dramatically illustrates the effect of small phase shifts in computing loops. The equation was also set up using a potentiometer in the loop, but no appreciable change occurred. This indicates that the

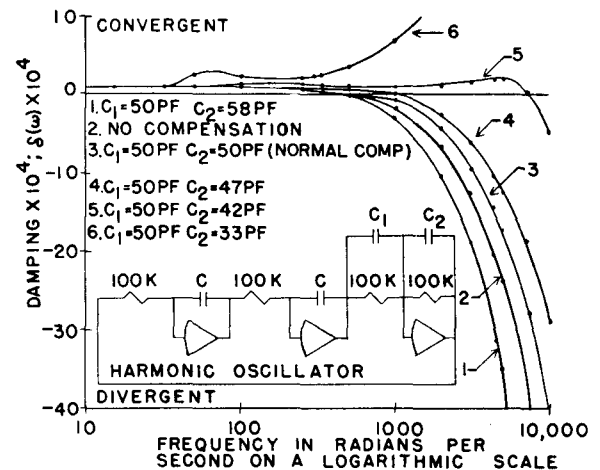


Fig. 18. — Damping characteristics of the ASTRAC I harmonic oscillator computer setup.

low-resistance potentiometers used in ASTRAC I do not contribute objectionable phase shift.

Experimental results and equivalent circuit studies of linear computing elements, indicate that dynamic errors are smaller if short leads and particularly, low computing impedances are used in conjunction with wide-band, high-gain, operational amplifiers [26]. To test this theory, the solution for the harmonic oscillator equation was simulated on ASTRAC I using 10K carbon resistors and very short wiring. The results are shown in figure 19, and vindicate the theory quite

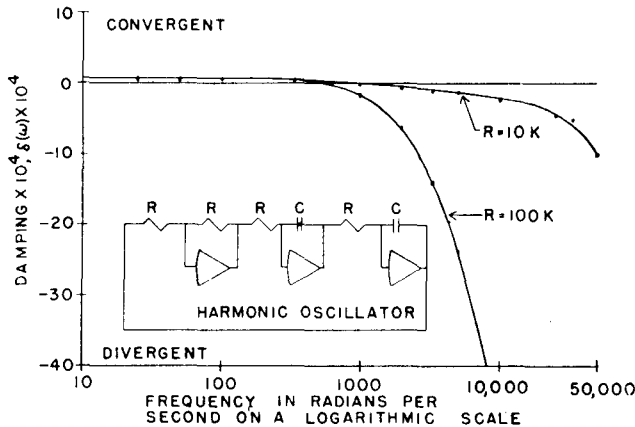


Fig. 19 — Damping characteristics for a low impedance and high impedance ASTRAC I harmonic oscillator computer setup.

well. The important thing to consider is that the use of low impedances permits the utilization of the complete amplifier band-width and amplifier limitations will be the determining factor in high frequency dynamic errors. Note that this also requires a high-current amplifier.

When a timed sampling readout is used to plot computer solutions, small frequency errors can cause large amplitude errors, as shown in figure 20. Here,

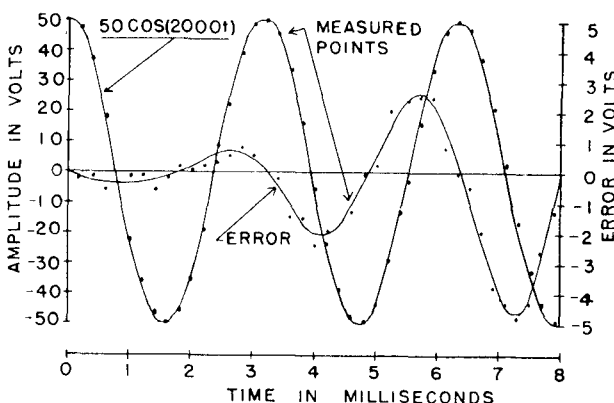


Fig. 20. — Amplitude error of timed samples due to a small frequency perturbation.

the experimental points indicate that the solution frequency is lower than the theoretical value and, although the experimental waveform is quite sinusoidal, the amplitude errors are large as the solution goes through

zero. To illustrate this further, consider the harmonic oscillator solution

$$x(t) = 100 \sin \omega t \quad (21)$$

where

$$\omega = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}} \quad (22)$$

For a one-percent error in R_1 , the resulting amplitude-time error is 3.14 volts per cycle as the solution goes through zero. Note that this error is the same for all frequencies.

In most simulations, this effect is not too important and can be treated as a small frequency perturbation. However, if amplitude errors are to be investigated from sample points, the effect of frequency error must be considered.

7. Effects of Timing Errors in the Digital Control Unit.

Errors in the digital control unit are caused by variations in the timing intervals due to the following causes:

1. Deviation of the oscillator frequency from 10 kc.
2. Delays due to « ripple-through-time » in the digital counters and digital circuits.

The crystal oscillator has a measured frequency of $9992.2 \pm .1$ cps, which results in a mean time interval of 0.10000785 msec. This alters each computing interval, but its greatest effect is on t_1 and t_2 timing. For example, if the computer solution

$$x(t) = 100 \sin (5000 t + \theta) \quad (23)$$

were to be sampled by presetting t_1 at 50 msec, the true sampling time would be 50.03925 msec, which gives a timing error of 0.03925 msec or 0.0785 percent. If the maximum rate of change of $x(t)$ is considered as constant over this time interval, the sample value would be in error by 19.625 volts or almost 20 percent of half-scale.

The delays of the various resetting pulses are tabulated in table 2. Table 3 shows the delays of the t_1 and t_2 sampling pulses with the 100 cps repetition rate used as a reference.

Although the oscillator frequency error is uniform, the sampling pulse time delays are not. To investigate this further, suppose the crystal oscillator frequency is exact and the only error is due to « ripple-through-delay ». If the waveform of equation (23) passes through zero at a theoretical time of 6 msec, and is sampled then by the t_1 sample-hold circuit, the delay error of 8.5 μ sec would cause the sample value to be in error by 4.25 volts.

Originally, the crystal oscillator was intentionally detuned for statistical studies; but in the near future, the addition of a commercial, temperature stabilized, crystal oscillator will permit the clock frequency to be set accurately at 10 kc. For most well designed experiments, even the fast repetition rate permits solutions of low enough frequency, so that the sampling delay errors are not too important. However, faster computers of this type will require transistorized digital control units which are designed using modern logic schemes. The delays in such control units will be in the order of tenths of microseconds.

Table 2
COMPUTER RESET
PULSE DELAY

Repetition rate in runs/second	Delay in $\mu\text{sec.}$
100	5.0
50	7.0
25	7.5
10	8.5

Table 3
SAMPLING PULSE DELAY

Note : All delays were measured with respect to the 100 cps repetition rate.

Samplin time in msec.	Delay in $\mu\text{sec.}$	Sampling time in msec.	Delay in $\mu\text{sec.}$
0.1	1.0	6.0	8.5
0.2	2.5	7.0	3.0
0.3	0.5	8.0	5.5
0.4	3.0	9.0	3.0
0.5	0.5	10.0	4.0
0.6	5.5	20.0	8.5
0.7	0.5	30.0	6.0
0.8	3.0	40.0	9.5
0.9	0.5	50.0	6.0
1.0	3.0	60.0	13.0
2.0	5.0	70.0	6.0
3.0	3.0	80.0	9.0
4.0	6.0	90.0	6.0
5.0	3.0		

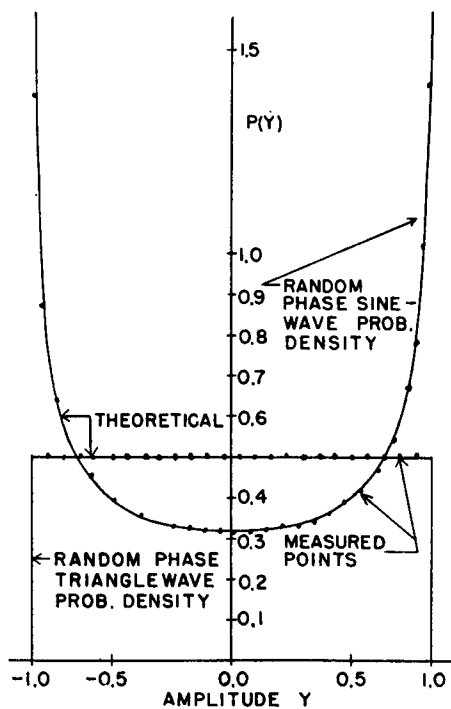


Fig. 21. — Probability densities for a random phase sine-wave and a random phase triangle-wave.

The above discussion vindicates the choice of a digital control system for ASTRAC I. It is questionable to generate accurate timing pulses using a comparator and a linear analog voltage. The analog signals simply are not accurate enough.

EXPERIMENTAL RESULTS : RANDOM-PROCESS STUDIES

1. Measurement of Cumulative Probability Distributions and Probability Densities.

Figure 21 shows normalized probability density functions for a random phase sine-wave and a random phase triangle-wave. Each waveform had an amplitude of 20 volts peak-to-peak.

The computer setup for generation of a Gaussian random variable, $x(t)$, and the measurement of the cumulative distribution function, $E[x(t)]$, and $E[x(t)^2]$

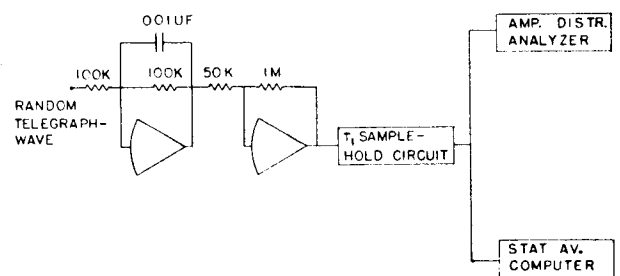


Fig. 22. — Computer setup for the measurement of the cumulative distribution function of gaussian noise.

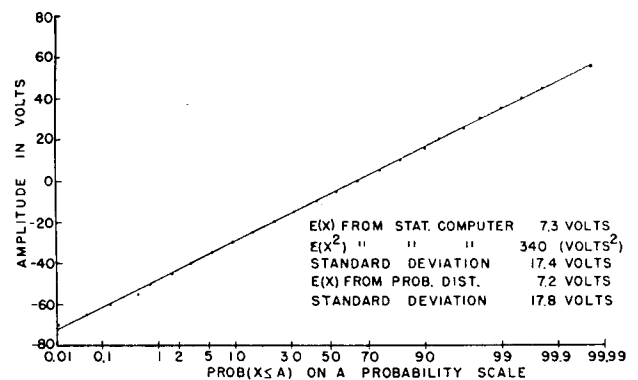


Fig. 23. — Cumulative distribution for gaussian noise generated by filtering a random telegraph wave.

is shown in figure 22. Figure 23 is a plot of the distribution function on probability paper along with tabulated values of the standard deviation and mean value. The curve indicates that the waveform is Gaussian to a good approximation.

2. Autocorrelation Function Measurements.

Conant has measured autocorrelation functions for Gaussian noise, Gaussian noise plus a sine-wave, and a random phase sine-wave [11]. The Gaussian noise was obtained by filtering a random telegraph wave. The computer setup used for the experiment is shown

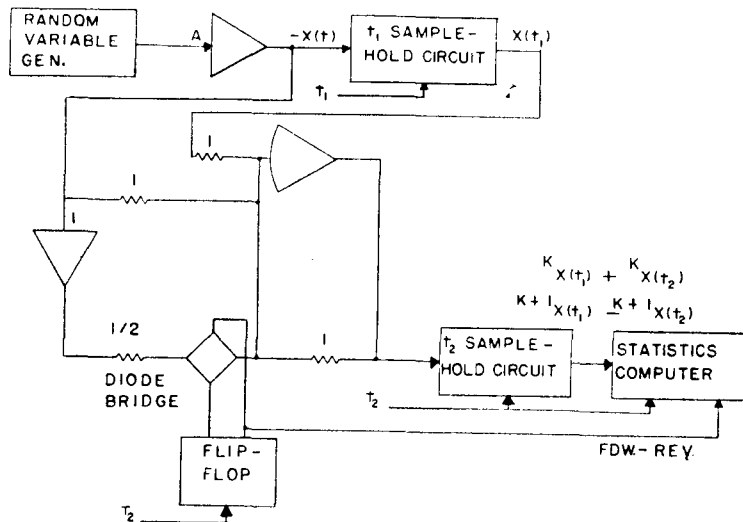


Fig. 24. — Computer setup for the measurement of auto-correlation functions.

in figure 24 and the results are plotted in figures 25, 26 and 27. An important result is that the Gaussian noise is essentially uncorrelated for samples separated by more than 5 msec in time.

3. Other Projects.

In addition to the problems discussed above, AS-TRAC I has worked on the following:

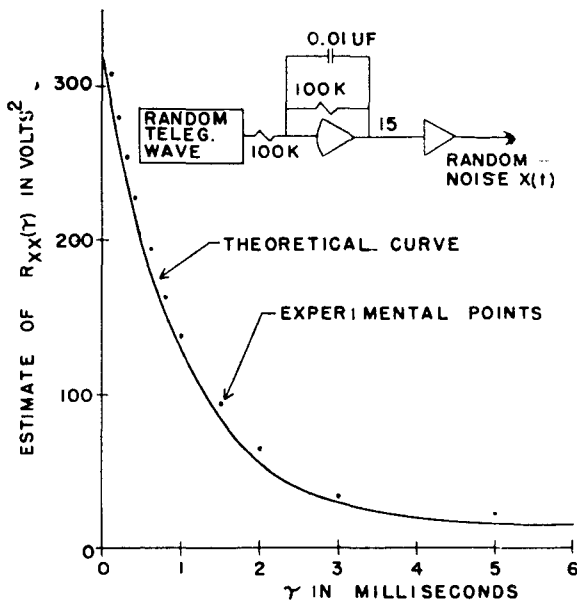


Fig. 25. — Autocorrelation function for gaussian noise generated by filtering a random telegraph wave.

1. Measurement of the mean-square of speech samples (Engineering Research Laboratory project).
2. Injection of artificial errors into alternate repetitive analog computer solutions (parameter perturbation; EE 272/3 term paper).
3. Simulation of steel-on-steel impact with analog memory techniques (Analog/Hybrid Computer Laboratory project).

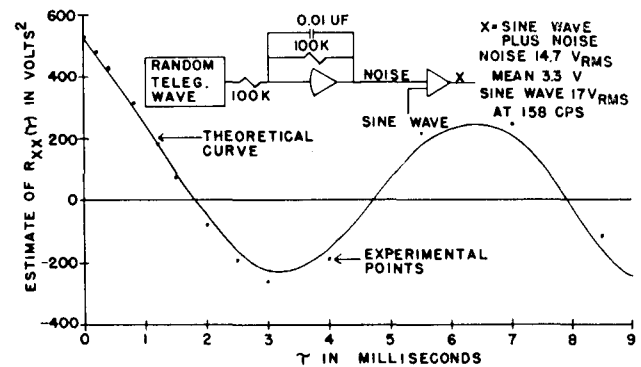


Fig. 26. — Autocorrelation function for a sine-wave plus noise.

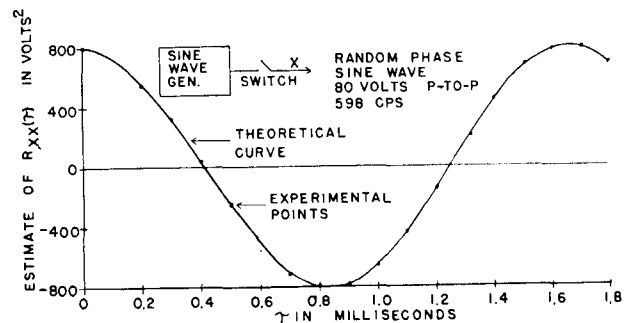


Fig. 27. — Autocorrelation function of a random phase sine-wave.

4. One-parameter automatic optimization by a new parameter perturbation method (solution of a boundary-value problem; Analog/Hybrid Computer Laboratory project).
5. Demonstration of a projectile trajectory with randomly disturbed initial conditions (Analog/Hybrid Computer Laboratory project).
6. Study of different optimization criteria for non-linear control systems with random-noise inputs [36].

Conclusions.

1. The ASTRAC I computer has proven to be a relatively accurate high-speed repetitive analog computer, which is well suited for studies of deterministic processes, stationary and non-stationary random processes, and parameter optimization. In addition, this new machine has already proved useful as a teaching aid illustrating the idea of ensemble statistics.
2. It appears feasible to construct all solid state repetitive analog computers to operate at a repetition rate of 1000 solutions per second, and at computing frequencies up to 50,000 radians per second. Figure 19 clearly indicates that this will require low computing impedances and wideband amplifiers with high current.

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